In re Patent Application of:
MAGRI' ET AL.
Serial No. **10/749,134**
Filing Date: **DECEMBER 30, 2003**

In the Claims:

Claims 1-23 (Cancelled).

24. (Previously Presented) A method for forming a vertical-conduction and planar-structure MOS device having a double thickness gate oxide, the method comprising:

forming spaced apart active areas in a semiconductor substrate and defining a JFET area therebetween, the JFET area also forming a channel between the spaced apart active areas;

forming a gate oxide on the semiconductor substrate and comprising

forming a first portion having a first thickness on the active areas and at a periphery of the JFET area, and

forming a second portion having a second thickness on a central area of the JFET area, the second thickness being greater than the first thickness; and

forming an enrichment region in the JFET area under the second portion of the gate oxide.

25. (Previously Presented) A method according to Claim 24, wherein the enrichment region is self-aligned with the second portion of the gate oxide.

26. (Previously Presented) A method according to Claim 24, wherein an interface between the first and second portions of the gate oxide has a tapered thickness.

27. (Previously Presented) A method according to Claim 24, further comprising the following steps after forming

the active areas:

forming an oxide pad on the active areas and on the channel;

forming a nitride layer on the oxide pad;

forming a photoresist layer on the nitride layer except over a portion of the JFET area corresponding to the second portion of the gate oxide;

removing the exposed nitride layer;

implanting dopants through the exposed oxide pad while using the photoresist as an implant window for forming the enrichment region in the JFET area; and

removing the photoresist layer.

28. (Previously Presented) A method according to Claim 27, wherein forming the gate oxide comprises:

growing the oxide pad for forming the first portion of the gate oxide layer;

removing the nitride layer;

selectively removing the first portion of the gate oxide layer on a central area of the active areas;

forming a sacrificial oxide layer on the first portion of the gate oxide layer;

removing the sacrificial oxide layer to expose a gate region on the channel; and

growing the first portion of the gate oxide layer on the gate region for forming the second portion of the gate oxide.

29. (Previously Presented) A method according to Claim 27, wherein the oxide pad has a thickness within a range

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of about 100 to 500 A; and wherein the nitride layer has a thickness with a range of about 300 to 900 A.

30. (Previously Presented) A method according to Claim 27, wherein the dopants comprise at least one of P, As and Sb ions for an N-channel transistor, and with the implanting being performed at an implant energy within a range of 60 to 900 KeV with ion doses ranging between 1E12 to 1E13 ions/cm^2.

31. (Previously Presented) A method according to Claim 27, wherein the dopants comprise at least one of B and Al ions for a P-channel transistor, and with the implanting being performed at an implant energy within a range of 60 to 900 KeV with ion doses ranging between 1E12 to 1E13 ions/cm^2.

32. (Previously Presented) A method according to Claim 24, further comprising the following steps after forming the active areas:

forming an oxide pad on the active areas and on the channel;

forming a polysilicon layer having a thickness less than or equal to one-half the second thickness of the second portion of the gate oxide;

forming a nitride layer on the polysilicon layer;

forming a photoresist layer on the nitride layer except over a portion of the JFET area corresponding to the second portion of the gate oxide;

removing the exposed nitride layer;

implanting dopants through the exposed polysilicon

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layer while using the photoresist layer as an implant window for forming the enrichment region in the JFET area;

removing the photoresist layer;

oxidizing the polysilicon layer not covered by the nitride layer;

removing the nitride layer; and

forming a gate electrode on the first and second portions of the gate oxide.

33. (Previously Presented) A method according to Claim 32, wherein the oxide pad has a thickness within a range of about 100 to 1500 A; and wherein the nitride layer has a thickness with a range of about 300 to 900 A.

34. (Previously Presented) A method according to Claim 32, wherein the dopants comprise at least one of P, As and Sb ions for an N-channel transistor, and with the implanting being performed at an implant energy within a range of 60 to 900 KeV with ion doses ranging between 1E12 to 1E13 ions/cm^2.

35. (Previously Presented) A method according to Claim 32, wherein the dopants comprise at least one of B and Al ions for a P-channel transistor, and with the implanting being performed at an implant energy within a range of 60 to 900 KeV with ion doses ranging between 1E12 to 1E13 ions/cm^2.

36. (Previously Presented) A method according to Claim 32, wherein the gate electrode comprises doped polysilicon.

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37. (Previously Presented) A method according to Claim 32, wherein the gate electrode comprises metal.

38. (Currently Amended) A method for forming a semiconductor device comprising:

forming spaced apart source and drain areas in a semiconductor substrate and defining a JFET area therebetween, the JFET area also forming a channel between the source and drain areas;

forming a gate oxide on the semiconductor substrate and comprising

forming a first portion having a first thickness on the source and drain areas and at a periphery of the JFET area, [[and]]

forming a second portion having a second thickness on a central area of the JFET area, the second thickness being greater than the first thickness, and

forming an enrichment region in the JFET area under the second portion of the gate oxide.

39. (Canceled).

40. (Previously Presented) A method according to Claim 38, wherein the enrichment region is self-aligned with the second portion of the gate oxide.

41. (Previously Presented) A method according to Claim 38, wherein an interface between the first and second portions of the gate oxide has a tapered thickness.

42. (Previously Presented) A method according to Claim 38, further comprising the following steps after forming the source and drain areas:

forming an oxide pad on the source and drain areas and on the channel;

forming a nitride layer on the oxide pad;

forming a photoresist layer on the nitride layer except over a portion of the JFET area corresponding to the second portion of the gate oxide;

removing the exposed nitride layer;

implanting dopants through the exposed oxide pad while using the photoresist as an implant window for forming the enrichment region in the JFET area; and

removing the photoresist layer.

43. (Previously Presented) A method according to Claim 42, wherein forming the gate oxide comprises:

growing the oxide pad for forming the first portion of the gate oxide layer;

removing the nitride layer;

selectively removing the first portion of the gate oxide layer on a central area of the source and drain areas;

forming a sacrificial oxide layer on the first portion of the gate oxide layer;

removing the sacrificial oxide layer to expose a gate region on the channel; and

growing the first portion of the gate oxide layer on the gate region for forming the second portion of the gate oxide.

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44. (Previously Presented) A method according to Claim 42, wherein the oxide pad has a thickness within a range of about 100 to 500 A; and wherein the nitride layer has a thickness with a range of about 300 to 900 A.

45. (Previously Presented) A method according to Claim 42, wherein the dopants comprise at least one of P, As and Sb ions for an N-channel transistor, and with the implanting being performed at an implant energy within a range of 60 to 900 KeV with ion doses ranging between 1E12 to 1E13 ions/cm^2.

46. (Previously Presented) A method according to Claim 42, wherein the dopants comprise at least one of B and Al ions for a P-channel transistor, and with the implanting being performed at an implant energy within a range of 60 to 900 KeV with ion doses ranging between 1E12 to 1E13 ions/cm^2.

47. (Previously Presented) A method according to Claim 38, further comprising the following steps after forming the source and drain areas:

forming an oxide pad on the source and drain areas and on the channel;

forming a polysilicon layer having a thickness less than or equal to one-half the second thickness of the second portion of the gate oxide;

forming a nitride layer on the polysilicon layer;

forming a photoresist layer on the nitride layer except over a portion of the JFET area corresponding to the

second portion of the gate oxide;

removing the exposed nitride layer;

implanting dopants through the exposed polysilicon layer while using the photoresist layer as an implant window for forming the enrichment region in the JFET area;

removing the photoresist layer;

oxidizing the polysilicon layer not covered by the nitride layer;

removing the nitride layer; and

forming a gate electrode on the first and second portions of the gate oxide.

48. (Previously Presented) A method according to Claim 47, wherein the oxide pad has a thickness within a range of about 100 to 1500 A; and wherein the nitride layer has a thickness with a range of about 300 to 900 A.

49. (Previously Presented) A method according to Claim 47, wherein the dopants comprise at least one of P, As and Sb ions for an N-channel transistor, and with the implanting being performed at an implant energy within a range of 60 to 900 KeV with ion doses ranging between 1E12 to 1E13 ions/cm^2.

50. (Previously Presented) A method according to Claim 47, wherein the dopants comprise at least one of B and Al ions for a P-channel transistor, and with the implanting being performed at an implant energy within a range of 60 to 900 KeV with ion doses ranging between 1E12 to 1E13 ions/cm^2.

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